

STR-X6400 Application

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1. Introduction

The STR-X6400 series is a hybrid IC with a built-in MOSFET and a control IC, designed for fly-back converter SMPS (Switching Mode Power Supply) applications. The IC is suitable for simplifying and standardizing power supply systems, by reducing the number of external components, and simplifying circuit designs. The IC is also applicable for Quasi-Resonant, low frequency PRC, and Burst mode at stand-by designs.

Note: PRC stands for Pulse Ratio Control (ON width Control with fixed OFF-time)

2. Features

- Newly developed SIP fully molded 7 pin package.
- Built-in Step-Drive circuit provides low noise switching.
- Built-in Bottom-Skip operation circuit operates from light to medium load ranges, and reduces switching losses.
- Built-in Intermittent Operation circuit provides an intermittent oscillation at light load, reducing input power.
- For protective functions, the STR-X6400 series has the same Overcurrent Protection (OCP), Overvoltage Protection (OVP), and Thermal Shutdown (TSD) as those of the former series. It also has Overload Protection (OLP); which operates as latch at over load in the secondary side, which reduces stresses on external components within the power supply and the IC itself.

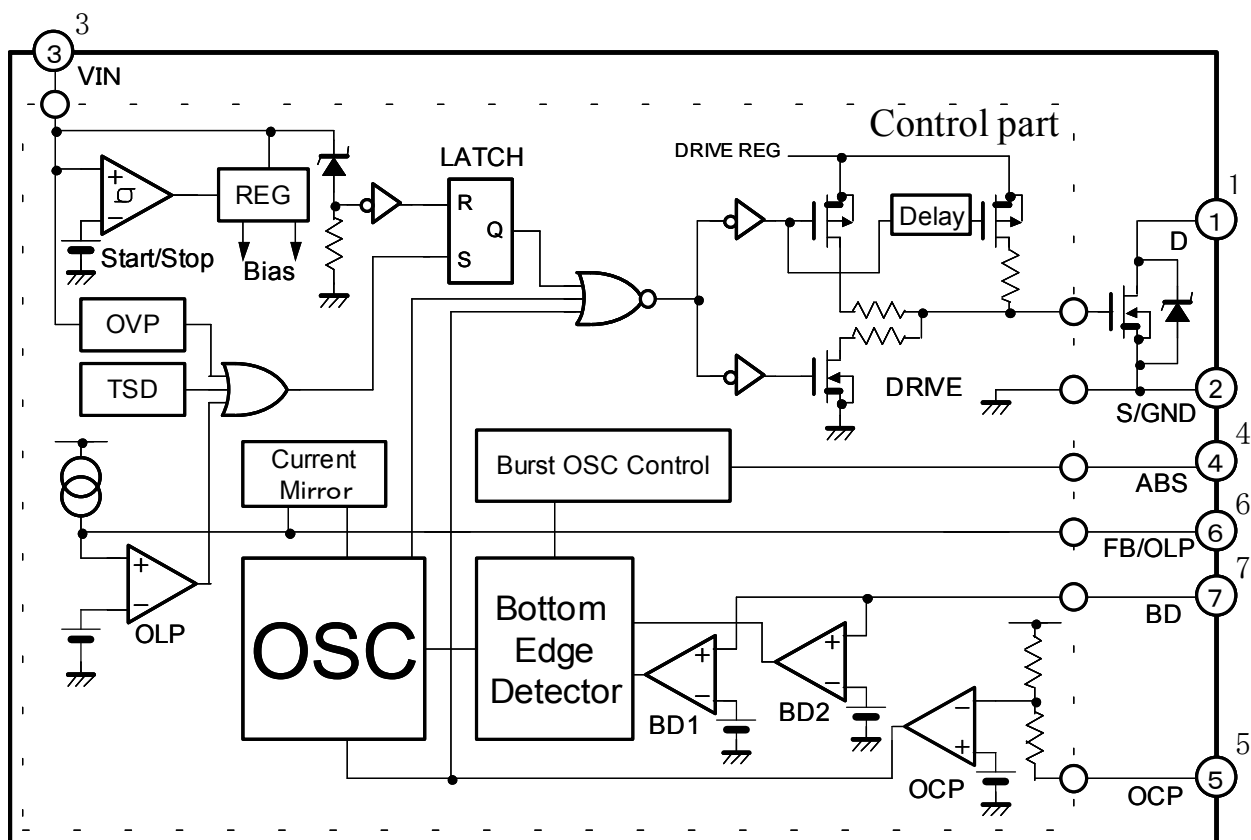
3. Line-up of STR-X6400 Series

Type *3	MOSFET V _{DSS} [V]	RDS(ON) MAX[ohms]	V _{AC} INPUT[V]	P _{out} [W] *1	T _{OFF} (MIN1)/ T _{OFF} (MIN2)[uS]		
STR-X6456	650	0.73	220	285	5.2/7.2		
			WIDE	144			
STR-X6468	800	1.00	220	240	6.0/8.0		
			WIDE	120			
STR-X6459	650	0.385			8.8/10.7		
			WIDE	300			

*1. The P_{out} (W) represents the thermal ratings, and the peak output power obtains by 120%~140% approximately. Where the output voltage is low and the ON-duty is narrow, the P_{out} (W) shall be smaller than that of above.

*2. Preliminary.

5. STR-X6400 Series Block Diagram



Terminal Functions

Terminal	Symbol	Description	Functions
1	D	Drain Terminal	MOSFET Drain
2	S / GND	Source / Ground Terminal	MOSFET Source / Ground
3	V _{IN}	Power Supply Terminal	Power Supply for Control Circuit
4	ABS	Stand-by Terminal	Stand-by Control
5	OCP	Overcurrent Protection Terminal	Overcurrent Detection Signal Input
6	FB/OLP	Feedback / Overload Protection Detecting Terminal	Overload Detection and Constant Voltage Control Signal Input
7	BD	Bottom Detecting Terminal	OFF-time Synchronization

6. Electrical Characteristics: STR-X6469 (Example)

Absolute Maximum Ratings (Ta = 25°C)

Description	Terminal	Symbol	Ratings	Unit	Remarks
Drain Current	1-2	$I_{D\ peak}^{*1}$	22	A	Single Pulse
Maximum Switching Current	1-2	$I_{D\ MAX}^{*2}$	22	A	Ta=-20~+125°C
Avalanche Energy Capacity	1-2	E_{AS}^{*3}	395	mJ	Single Pulse
					VDD=30V, L=50mH IL=3.9A
Input Voltage to Control Part	3-2	V _{IN}	35	V	
FB/OLP Terminal Current	6-2	I _{FBOLP}	3	mA	
OCP Terminal Voltage	5-2	V _{OCP}	-1.5~5	V	
BD Terminal Voltage	7-2	V _{BD}	-0.5~6	V	
ABS Terminal Voltage	4-2	V _{ABS}	-0.5~6	V	
Power Dissipation at MOSFET	1-2	P _{D1} ^{*4}	46	W	With Infinite Heat Sink
			2.8		Without Heat Sink
Power Dissipation at Control Part (MIC)	3-2	P _{D2} ^{*5}	0.8	W	V _{IN} × I _{IN}
Internal Frame Temp. at Operation	-	T _F	-20~+125	°C	Refer to Recommended Operating Temperature
Operating Ambient Temp.	-	T _{op}	-20~+125	°C	
Storage Temperature	-	T _{stg}	-40~+125	°C	
Channel Temperature	-	T _{ch}	+150	°C	

*1. Refer to the MOSFET S.O.A. curve on the specifications.

*2. Refer to the Maximum Switching Current on the specifications. The Maximum Switching Current is the drain current determined by both the drive voltage of the IC and the V_{th} of the MOSFET.

*3. Refer to the MOSFET T_{ch}-E_{AS} curve on the specifications.

*4. Refer to the MOSFET Ta-PD₁ curve on the specifications.

*5. Refer to the MIC T_F-PD₂ curve on the specifications.

Note: Refer to the specifications for details since the values are different for each product.

Electrical Characteristics of Control Part (Ta=25°C) (Example: STR-X6469)

Parameter	Terminal	Symbol	Ratings			Unit	Conditions
			MIN	TYP	MAX		
Operation Start Voltage	3-2	V _{IN(ON)}	16.3	17.9	19.9	V	*9
Operation Stop Voltage	3-2	V _{IN(OFF)}	9.3	10.2	11.1	V	
Circuit Current at Operation	3-2	I _{IN(ON)}	-	-	8	mA	
Circuit Current at Non-Operation	3-2	I _{IN(OFF)}	-	-	100	μA	
Maximum OFF-Time	-	T _{OFF(MAX)}	41.0	47.0	52.5	μsec	
Minimum OFF-Time 1 *6	-	T _{OFF(MIN1)}	5.4	6.0	6.8	μsec	
Minimum OFF-Time 2 *6	-	T _{OFF(MIN2)}	7.0	8.0	9.0	μsec	
OCP Terminal Threshold Voltage	5-2	V _{OCP}	-0.99	-0.89	-0.79	V	
OCP Terminal Current	5-2	I _{OCP}	70	160	340	μA	
BD Terminal Threshold Voltage 1	7-2	V _{BD(1)}	0.4	0.5	0.6	V	
BD Terminal Threshold Voltage 2	7-2	V _{BD(2)}	1.0	1.2	1.4	V	
BD Terminal Input Current	7-2	I _{BD}	-100	-	100	μA	
Stand-by Mode Switching Time 1 *6	-	T _{STB(1)}	2.1	2.8	3.6	μsec	
Stand-by Mode Switching Time 2 *6	-	T _{STB(2)}	5.2	6.7	8.7	μsec	
ABS Terminal Threshold Voltage 1	4-2	V _{ABSTH(1)}	0.85	1.0	1.15	V	
ABS Terminal Threshold Voltage 2	4-2	V _{ABSTH(2)}	2.8	3.1	3.4	V	
ABS Terminal Charging Current	4-2	I _{ABS(OUT)}	135	165	195	μA	
ABS Terminal Discharging Current	4-2	I _{ABS(IN)}	10	14	18	μA	
FB/OLP Terminal Threshold Voltage	6-2	V _{OLP}	6.8	7.2	7.7	V	
FB/OLP Terminal Current	6-2	I _{OLP}	70	105	135	μA	
OLP Delay-Time	6-2	T _{OLP}	20	40	60	ms	
OVP Operating Voltage	3-2	V _{IN(OVP)}	25.5	27.5	29.8	V	
Latch Circuit Holding Current *7	3-2	I _{IN(H)}	-	-	170	μA	
Latch Circuit Releasing Voltage *7	3-2	V _{IN(La.OFF)}	8.0	9.0	10.5	V	
TSD Operating Temperature *8	-	T _{J(TSD)}	140	-	-	°C	-

*6 Refer to the specifications for details.

*7 Latch Circuit represents the circuit operated by OVP, TSD, and OLP.

*8 Reference value.

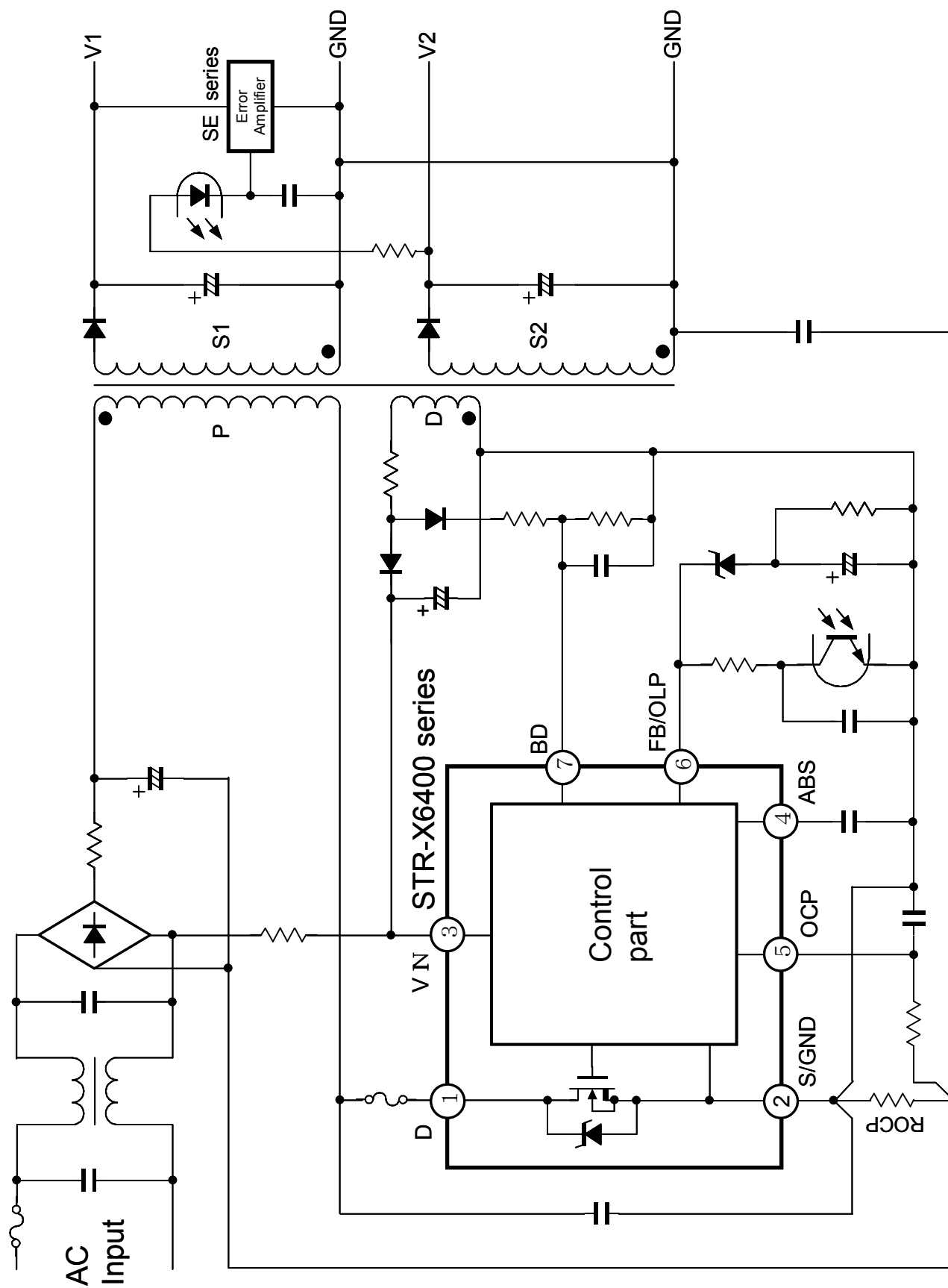
*9 Refer to the specifications for details since the values are different for each product.

Electrical Characteristics of MOSFET (Ta=25°C) (Example: STR-X6469)

Parameter	Terminal	Symbol	Ratings			Unit	Conditions
			MIN	TYP	MAX		
Drain to Source Breakdown Voltage *10	1-2	V _{DSS}	800	-	-	V	*10
Drain Leakage Current	1-2	I _{DSS}	-	-	300	μA	
ON-Resistance *10	1-2	R _{DS(ON)}	-	-	0.66	ohms	
Switching Time	1-2	t _f	-	-	400	nsec	
Thermal Resistance *10	-	θ _{ch-F}	-	-	0.99	°C/W	Channel - Internal Frame

*10 Refer to the specifications for details since the values are different for each product.

7. Application Circuit



8. Functions of Each Terminal and Operation

8.1. VIN Terminal (Pin 3)

8.1.1. Start-up Circuit

The start-up circuit detects the voltage at the VIN terminal (Pin 3), and the circuit starts and stops the operation of the control IC. The power supply circuit (VIN terminal input) of the control IC employs a circuit as shown in Fig.1. At start-up of the power supply, C3 is charged through the start-up resistor R2. The R2 value should be selected to limit the current to no less than the holding current of the latch circuit (170μA MAX), which will be described later, to flow at the minimum AC input voltage.

However, when the R2 value is too large, the current charging C3 after AC input will be reduced. Thus, a longer time is required to reach the start voltage.

The VIN terminal voltage falls immediately after the control circuit starts its operation, but the voltage drop ratio is reduced by increasing the C3 capacitance. Therefore, when the drive winding voltage is delayed in rising, the VIN terminal voltage does not reach the operational stop voltage to maintain start-up operation. However, if C3 capacitance is too large, the time after AC input for operation start becomes longer since it takes longer to charge C3.

In general, a power supply operates with C3 values between 22~100μF, and the R2 values of 33kΩ~100kΩ for wide input range of 100V, and 82kΩ~330kΩ for 200V input for start-up.

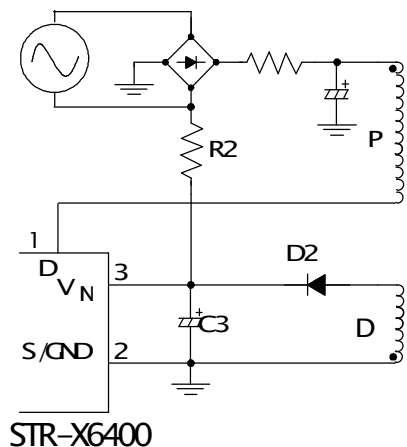


Fig.1. Start-Up Circuit

As shown in Fig.2, circuit current, before control circuit start-up, is regulated at maximum **100μA MAX**(VIN=15V, Ta=25°C), and the higher value resistance Rs is applicable.

The control circuit starts its operation via the **Start-Up Circuit**, as soon as the VIN terminal voltage reaches **17.9V(TYP)**, at which point the current consumption increases.

When the VIN terminal voltage drops lower than **10.2V(TYP)**, the **Under Voltage Lock Out (UVLO)** function stops the control operation, and returns to the start-up mode.

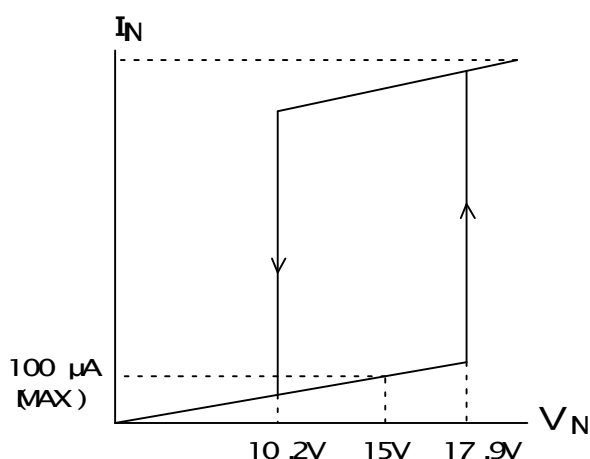


Fig.2. VIN Terminal Vol. - Circuit Cur. IIN

8.1.2. Drive Windings

After the control circuit starts its operation, drive winding D voltage, which being rectified, provides power to the IC.

Fig.3 shows the start-up voltage waveform of the V_{IN} terminal.

The drive winding voltage does not rise up to the set voltage immediately after the control circuit starts its operation, and the V_{IN} terminal voltage starts falling. Because the operational stop voltage is set as low as 11.1V(MAX), the drive winding voltage reaches stabilized voltage before falling to the operational stop voltage, and the control circuit continues operation.

The correct drive winding voltage, during normal power supply operation, results from setting the number of the windings so that the final voltage of C3 shall be higher than the operational stop voltage [$V_{IN}(\text{OFF})$ 11.1V(MAX)] and lower than the OVP operating voltage [$V_{IN}(\text{OVP})$ 25.5V (MIN)].

In an actual power supply circuit, there may be a case where the V_{IN} terminal voltage varies due to the value of secondary output current as shown in Fig.4. This is due to the low current of the STR-X6400, because the C3 is charged up to the peak value by the surge voltage generated after the MOSFET is turned OFF.

In order to prevent this, add a resistor having several ohms to several tens of ohms (R7) in series with the rectifier diode as shown in Fig.5. The optimum resistance value of this additional resistor should be determined in accordance with the specs of a transformer, since the V_{IN} terminal voltage is varied by the structural differences of the transformer.

Furthermore, the variation of the V_{IN} terminal voltage becomes worse due to an inaccurate coupling between the primary and the secondary winding of the transformer (the coupling between the drive winding D and the stabilizing output winding for the constant voltage control). Thus, in designing the transformer, drive winding D should be carefully designed.

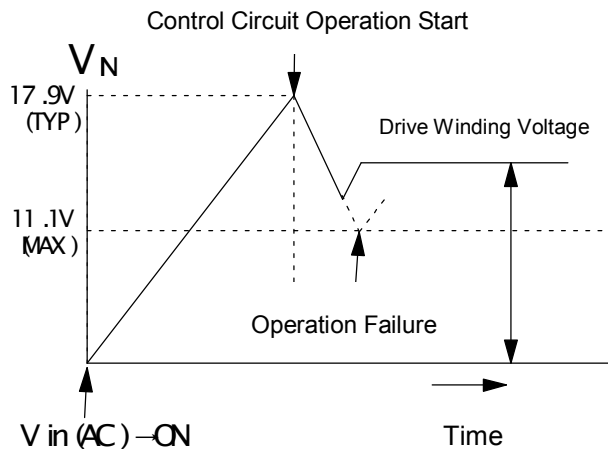


Fig.3. Waveform of V_{IN} Terminal Vol. at Start-Up

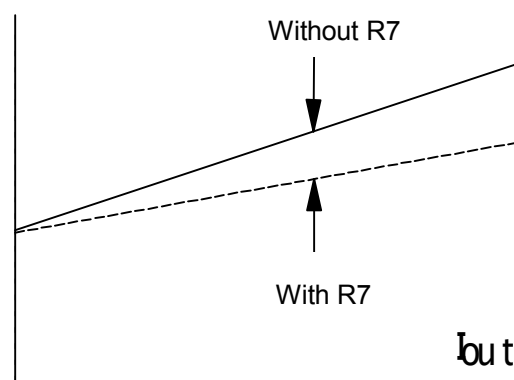


Fig.4. Output Current I_{OUT} - V_{IN} Terminal Vol.

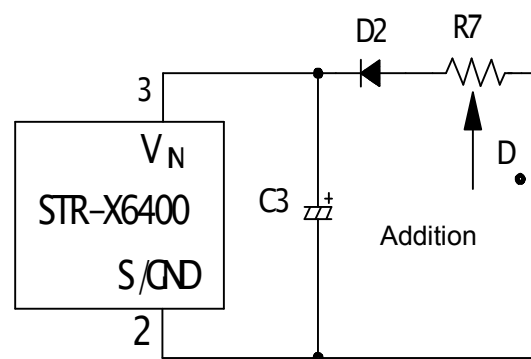


Fig.5. Effective Auxiliary Power Supply Circuit to Output Current I_{OUT}

8.1.3. Overvoltage Protection Circuit

When the voltage exceeds 27.5V (TYP) across the V_{IN} and the GND terminals, the OVP circuit of the control IC operates, providing a latch mode, which stops its oscillation.

Generally, the V_{IN} terminal voltage is supplied from the drive winding of the transformer, and the voltage is proportioned with the output voltage; thus, the circuit also operates at the overvoltage output in the secondary side, such as in the case of the voltage detection open circuit.

In this case, the secondary output voltage when the overvoltage protection circuit operates is obtained from the formula shown below.

$$V_{OUT} (OVP) \doteq \frac{V_{OUT} \text{ at Normal Operation}}{V_{IN} \text{ Terminal Voltage at Normal Operation}} \times 27.5V (TYP) \quad \cdots \cdots (1)$$

8.1.4. Latch Circuit

The Latch Circuit is a circuit holds the oscillator output low, and stops the power supply circuit operation when the OVP, TSD, or OLP circuits operate. The holding current of the latch circuit is 170 μ A MAX ($T_a=25^{\circ}\text{C}$) when the V_{IN} terminal voltage is minus 0.3V below the operational stop voltage.

In order to avoid malfunction caused by noise, the delay time is set by a timer circuit incorporated in the IC. Thereafter, the latch circuit starts operation when the OVP, TSD, or OLP circuits operate longer than the set time. The V_{IN} terminal voltage, however, will drop even after the latch circuit starts its operation, because the constant voltage (Reg.) circuit of the control circuit continues operation and maintains higher circuit current.

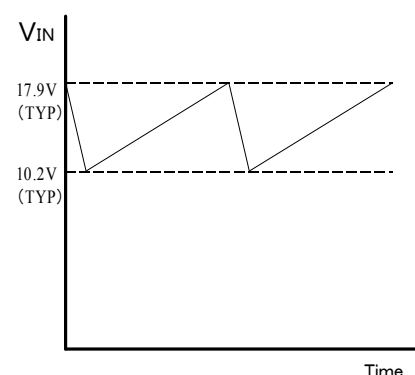


Fig.6. V_{IN} terminal Vol. Waveform
at Latch Circuit ON

Where the V_{IN} terminal voltage falls lower than the operation stop voltage (10.2V TYP), the voltage starts rising as the circuit current becomes below 170 μ A ($T_a=25^{\circ}\text{C}$). Where the V_{IN} terminal voltage reaches the operation start voltage (17.9V TYP), it falls as the circuit current is increased again. Consequently, the latch circuit prevents the V_{IN} terminal voltage from rising abnormally by controlling the voltage between 10.2V (TYP) and 17.9V (TYP).

The Fig.6 shows the voltage waveform when the latch circuit is in operation. The cancellation of the latch circuit is made by reducing the V_{IN} terminal voltage below 9V, and generally, it is restarted by AC input switch-off of the power supply.

8.2 OCP Terminal (Pin 5)

8.2.1 Minus Detecting Type

The OCP circuit in the STR-X6400 series is a pulse-by-pulse type that detects the peak drain current of the MOSFET every pulse and reverses the oscillator output.

As shown in Fig.7, the overcurrent detecting resistors R5, R4, and capacitor C5 are added as external components. The external components, R4 and C5, form a filter circuit to prevent surge current when the MOSFET is turned ON. The OCP circuit is to turn OFF the MOSFET when the OCP terminal voltage reaches the V_{OCP} , due to the voltage generated in overcurrent detecting resistor R5, when the switching current flows into the MOSFET at turn-ON.

The threshold voltage V_{OCP} of the OCP terminal is set at $-0.89V(TYP)$. The OCP circuit employs the minus detecting circuit, hence voltage V_3 inside the MIC is created by dividing the voltage between V_1 and R_5 with divider RB_1 , RB_2 , and R_4 .

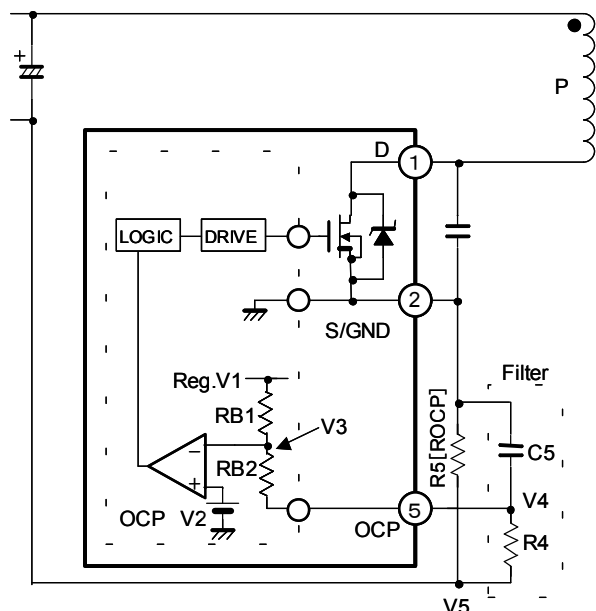


Fig.7. Minus Detecting Type OCP Circuit

Since the RB1 and RB2 are resistors inside the IC, the tolerance (rated as I_{OCP} for the products) of those resistors is important, and its effects are minimized by using the smaller value for R4 (100Ω etc).

8.2.2 Notes for OCP Circuit

The OCP circuit needs to be designed with consideration to the tolerance spread of $R_{OCP}(R5)$, V_{OCP} , and I_{OCP} . The tolerance of the OCP circuit (MAX/MIN of the drain current) is indicated as shown below:

$$\text{Drain Current MAX} \Rightarrow \text{Detecting Resistor } R_{OCP \text{ MIN}}, V_{OCP \text{ MIN}}, I_{OCP \text{ MAX}} \quad \cdots \cdots (2)$$

$$\text{Drain Current MIN} \Rightarrow \text{Detecting Resistor } R_{OCP \text{ MAX}}, V_{OCP \text{ MAX}}, I_{OCP \text{ MIN}} \quad \dots\dots(3)$$

To examine the above conditions, the samples of V_{OCP} MIN or I_{OCP} MAX are not to be made; therefore formula (2) and (3) are to be studied with calculating the R_{OCP} ' from below formula (4) and (5), and by applying the R_{OCP} ', V_{OCP} and I_{OCP} with measuring the value experimentally.

$$\text{Drain Current MAX} \Rightarrow R_{OCP}' = \frac{V_{OCP}(S)}{V_{OCP}(MIN)} \times R_{OCP} \times 0.95 \times \frac{|V_{OCP}(S)| + R_4 \times I_{OCP}(S)}{|V_{OCP}(S)| + R_4 \times I_{OCP}(MAX)} \quad \dots\dots(4)$$

$$\text{Drain Current MIN} \Rightarrow R_{OCP}' = \frac{V_{OCP}(S)}{V_{OCP}(MAX)} \times R_{OCP} \times 1.05 \times \frac{|V_{OCP}(S)| + R_4 \times I_{OCP}(S)}{|V_{OCP}(S)| + R_4 \times I_{OCP}(MIN)} \quad \dots\dots(5)$$

*Consider the distribution of: VOCp R5 IOPp

VOCp(S), IOCP(S): The measured value of the samples; VOCp, IOCP. Refer to the measured circuit 2 on the specs for the measuring. In case the samples measured values are required, please contact your

nearest Sanken sales office.

ROCP: Assuming the typical value of the OCP resistor R5 as $\pm 5\%$ for the ROCP distributions.

The distribution of R4 is negligible since its effect is minor.

The OCP circuit can be studied with the distributions (VOCP, IOCP, and ROCP) by employing the samples measured value and ROCP' experimentally.

8.2.3 Overload

The output characteristics of the secondary side, when the OCP circuit operates due to the overload of the secondary side output, are shown in Fig.8. The output voltage drops with overload, the drive winding voltage of the primary side also falls proportionally, and the VIN terminal voltage falls below shutdown voltage to stop the operation. In this case, as the circuit current also decreases simultaneously, and VIN terminal voltage rises by the Rs charging current, and the circuit re-operates intermittently, at the operational start voltage.

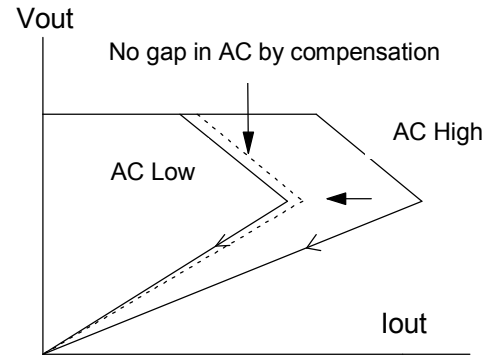


Fig.8. Power Supply Output Overload Characteristics

However, where a transformer has many output windings and the coupling is not sufficient, and even if the secondary output voltage drops in overload mode, the operation may not be intermittent because the primary winding voltage does not drop. Although the intermittent operation may not occur, protection can be provided by the OLP circuit, as described later.

8.2.4 Compensation Circuit of Input for OCP Circuit

In the STR-X6400 series, the OCP detects the peak value of the drain current of the MOSFET; therefore when the input voltage is large, the output voltage is increased at protection circuit operation, as shown in Fig.8.

In order to prevent this, it is effective to lay out the circuit as shown in Fig.9 (resistor RH), and add a bias in proportion to the input voltage. The compensation is provided by dividing the voltage (VD) generated at the drive winding D with R4 and RH, and combining the voltage in proportion to the input voltage of the OCP terminal. In this case, assuming the voltage generated when the MOSFET is turned ON as VD, the voltage generated at R4 as VR4, and the voltage generated at ROCP[R5] as VROCP; then the V4 voltage imposed on the OCP terminal is compensated as shown below.

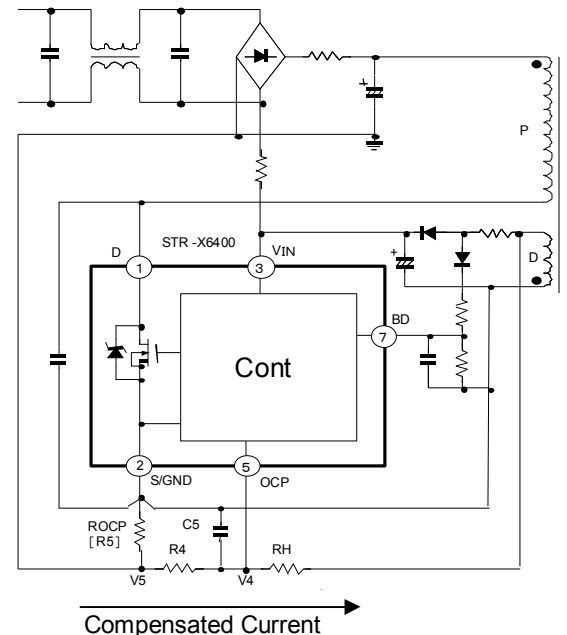


Fig.9. OCP Compensation Circuit (6)

$$V4 = VROCP + VR4 = VROCP + VD \times \frac{R4}{R4 + RH}$$

$$VD = (\text{Voltage} \cdot \text{Input} \cdot \text{after} \cdot \text{smoothing} \cdot AC) \times \frac{(\text{Winding} \cdot \text{No.} \cdot \text{of} \cdot VD)}{(\text{Winding} \cdot \text{No.} \cdot \text{of} \cdot \text{Primary} \cdot \text{Windings})} \dots\dots(7)$$

Where the R4 is 100Ω, normally the RH is 8.2k~22kΩ. The drain current, which is overloaded even if the input voltage is low, shall be decreased due to this compensation.

The formula (6) does not include that the AC voltage and the peak value of the drain current, which are not in proportion to the voltage drop of R4 x I_{OCP}; therefore, each fixed number needs to be adjusted in order to set the correct operating point of the OCP circuit, as calculated from formula (6).

There are two advantages to adding this external circuit:

- 1). When the input voltage is large, the drain current of the MOSFET is controlled at low level; thus the voltage stress to the MOSFET at start-up and at light load is also reduced by lowering the surge voltage caused by the transformer.
- 2). The current stress to the rectifier diodes of the secondary side is reduced since the output power is controlled.

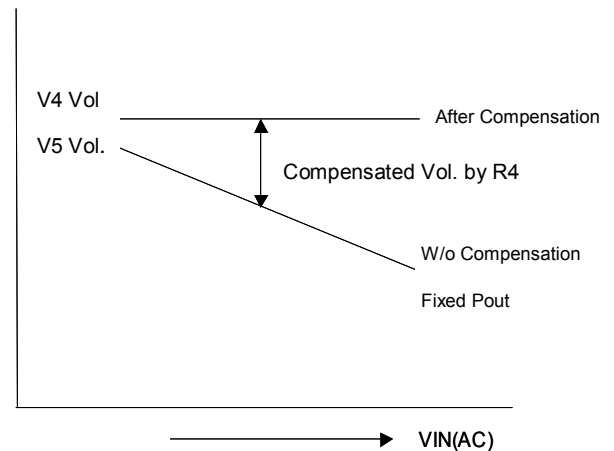


Fig.10. Compensation for OCP Operation Point to Input Voltage

8.3 FB/OLP Terminal (Pin 6)

The operation of FB/OLP terminal can be divided into; (1) at normal operation (constant voltage control circuit operation), (2) at overload operation, and at (3) power OFF.

8.3.1 Constant Voltage Control Circuit

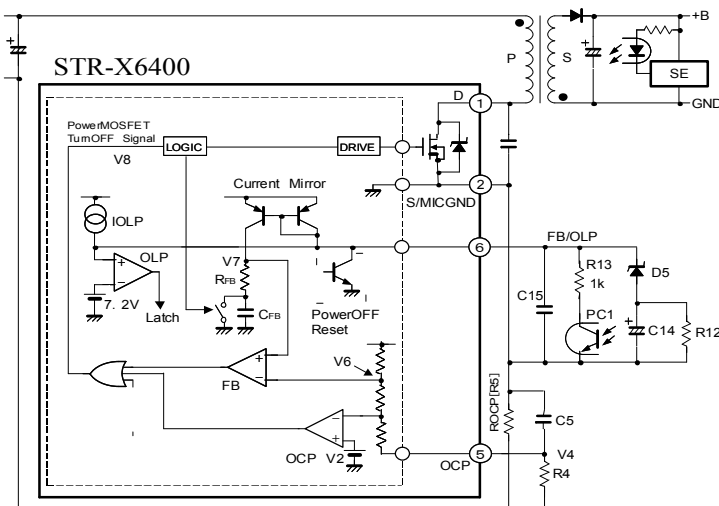


Fig.11. Constant Voltage Control Circuit

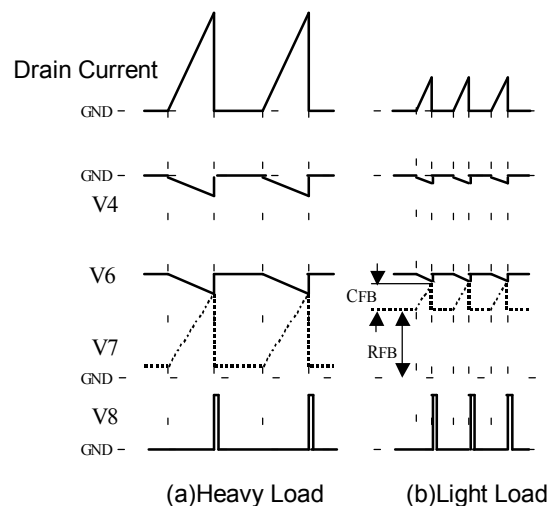


Fig.12. Timing Chart of Constant Voltage Control

The constant voltage control is made by varying the ON-time of the MOSFET, which is applied as the charging time to the internal CFB of the IC. During OFF-time, Quasi-Resonant operation synchronized with the reset signal from a transformer is applied. When there is no reset signal from the transformer, the OFF-time is determined by the PRC operation, which fixes the OFF-time by the internal oscillating circuit of the IC. The block diagram at the constant voltage control is shown in Fig.11, and Fig.12 shows the timing chart.

The constant voltage control uses the control signal (FB current) flowing from the secondary side error-amplifiers(SE) into the No.6 terminal by PC1. The FB current is input to RFB, CFB, and FB comparator through the internal current mirror circuit of the IC, and the input terminal of the FB comparator, the voltage waveform, which reversed drain current, is to the input. In the overload mode, as shown in Fig.12(a), the charging current to the CFB is decreased as the FB current decreases, and it lengthens the ON-width. During this interval, the control IC is protected by combining the current inputs to the FB comparator. While in the light load mode, as shown in Fig.12(b), the ON-width decreases as the charging current to the CFB increases with increasing the FB current. Due to the bias through RFB, the circuit is laid out to restrict the rapid increase of the FB current.

8.3.2 Constant Voltage Control and OLP Circuit

The IOLP current (105 μ A TYP) at the constant voltage control flows into the photo-coupler PC1 along with the FB current. The IOLP current (105 μ A TYP) is supplied at the constant current circuit; therefore where the photo-coupler PC1 value is goes below IOLP, the terminal voltage is 3.1V approx. The current flowing to the photo-coupler is:

At large load: IOLP+FB current (several tens μ A approx.) = 100~200 μ A approx.(8)

At medium load: IOLP+FB current (200 μ A approx.) = 200~400 μ A approx.(9)

At small load: IOLP+FB current (several hundreds μ A approx.) = 400~800 μ A approx.(10)

When the OLP operates, as shown in Fig.11, a Zener diode D5 and a capacitor C14 are to be connected in series to control the transient response at normal operation. A Zener diode having hard-break characteristics should be selected, and for the normal application, 5.6B (Rohm etc.) is recommended.

8.3.3 Overload Operation

The output voltage of secondary side drops in the overload mode (when drain current is controlled by the OCP operation), and the error- amplifier of the secondary side and the photo-coupler PC1 are cut off. As a result of this, the FB/OLP terminal voltage starts increasing by IOLP as shown in Fig.13, and when the FB/OLP terminal voltage reaches VOLP (7.2V TYP), the oscillation stops and it switches the operation to the latch protection mode.

Since the IOLP is the constant current circuit, the time to the latch protection can be calculated from:

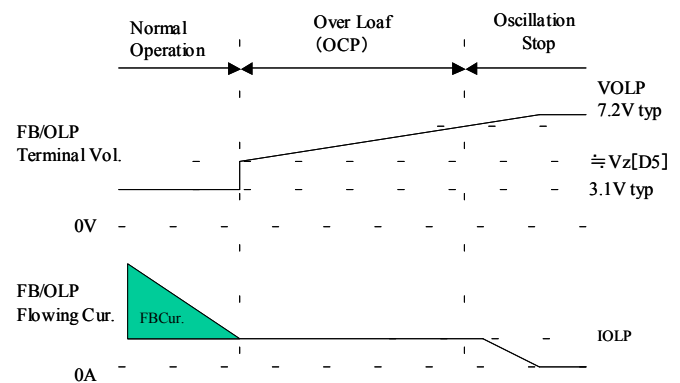


Fig.13. Timing Chart at Overload

$$C14 \text{ (Capacity of the Condenser)} \times \Delta V \text{ (Electrolytic Capacitor Charging Voltage)} = I \text{ (IOLP current value)} \times t \text{ (Time)} \dots\dots(12)$$

Due to the voltage dependency characteristics of the FB/OLP terminal voltage, the IOLP decreases while the FB/OLP terminal voltage increases. The application should be studied carefully, considering the actual load conditions, since the actual value and the value from the formula (12) may not match completely. Furthermore, at the start-up of the power supply, since the photo-coupler is cut off and the FB current value approaches zero, latch protection operation needs to be confirmed.

8.3.4 Operation at Power OFF

Fig.14 shows the reset circuit. The capacitor is discharged by the internal reset circuit of the IC at power OFF. The reset circuit does not start its operation while the internal constant voltage circuit is operating.

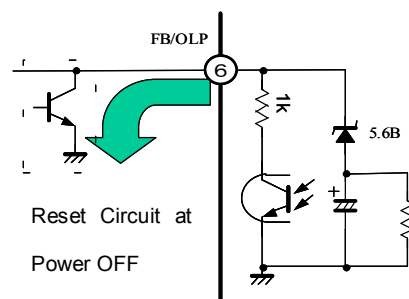


Fig.14. Reset Circuit

8.3.5 Notes for Additional Circuit

Once the power is turned ON, this OLP circuit does not have the discharging route from the additional capacitor.

Therefore, there may be a case where the OLP circuit operates even in the intermittent OCP operation. In order to provide a discharging path, the discharging resistor is to be connected in parallel with the capacitor. The value of the resistor is 100k~220kΩ approx, assuming 5~20% of I_{OLP} is diverted.

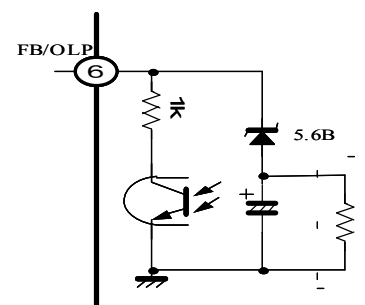


Fig.15. Discharging Resistance Circuit

8.3.6 Cancellation of OLP Circuit

At overload or start-up mode, the OLP operation is cancelled by inserting the Zener diode having 5.6B between the FB/OLP terminals.

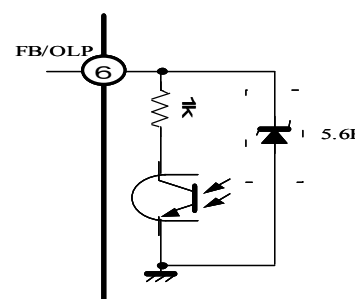


Fig.16. OLP Cancellation Circuit

8.4 Quasi-Resonant and Bottom-Skip Operation

8.4.1 Quasi-Resonant operation and BD Terminal

The Quasi-Resonant operation matches the timing of the MOSFET turn-ON to the bottom point of the voltage resonant waveform after a transformer releases the energy (i.e., 1/2 cycle of the resonant-frequency).

As shown in the Fig.17, the voltage resonant capacitor C4 is connected between the Drain and the Source terminal, and the delay circuit C10, D3, R9, and R10 are to be connected between the drive winding D and the BD terminal (No.7). When the MOSFET is turned OFF, the Quasi-Resonant signals, which are derived from the fly-back voltage generated at the drive windings, operate both the internal BD1 and 2 of the IC, which provides the Quasi-Resonant operation.

Due to the operation of the delay circuit, even if the energy release from the transformer is completed, the Quasi-Resonant signals imposed on the No.7 terminal do not drop immediately. This is because C10 is discharged by R10, and after a set period, the voltage drops to the threshold voltage $V_{BD(1)} \doteq 0.5V$ and below. Consequently, the delay time is to set by adjusting C10 while monitoring the operating waveform, and the delay time is set to allow the MOSFET to turn ON when the V_{DS} of the MOSFET is at its lowest level.

In addition to this Quasi-Resonant operation, to allow control of the oscillating frequency at light to medium load, there is a built-in Bottom-Skip function, which increases the OFF-time in accordance with the load (Refer to Fig.21). The timing between the Quasi-Resonant and the Bottom-Skip shall be described below.

When the Quasi-Resonant signal voltage imposed on the BD terminal is below $V_{BD(2)} \doteq 1.2V$, the internal oscillation circuit starts the ON-time controlled PRC operation with the fixed OFF-time ($T_{OFF} \doteq 46\mu sec$).

The PRC operation occurs when drive winding voltage is low, such as in start-up mode or short-circuit, and reduces current stress in the MOSFET as the frequency decreases. When the voltage is above $V_{BD(2)} \doteq 1.2V$ (6.0V MAX) or over, the internal oscillation circuit operates, and switches the OFF-time to either $T_{OFF(MIN1)}$ or $T_{OFF(MIN2)}$, and it fixes the OFF-time during this period. When the voltage is held higher than $V_{BD(1)} \doteq 0.5V$ after it exceeds the $V_{BD(2)} \doteq 1.2V$, the MOSFET will remain OFF. Thus it prevents malfunction with the voltage difference of $V_{BD(1)}$ and $V_{BD(2)}$.

Since the voltage imposed on the BD terminal is 6V (MAX), the Quasi-Resonant signals to the BD terminal are to be set below that voltage. The impedance of internal comparator is higher compared to that of the conventional STR-F6600 series; therefore the loss from the resistor is reduced by using higher resistor value for R9 and R10.

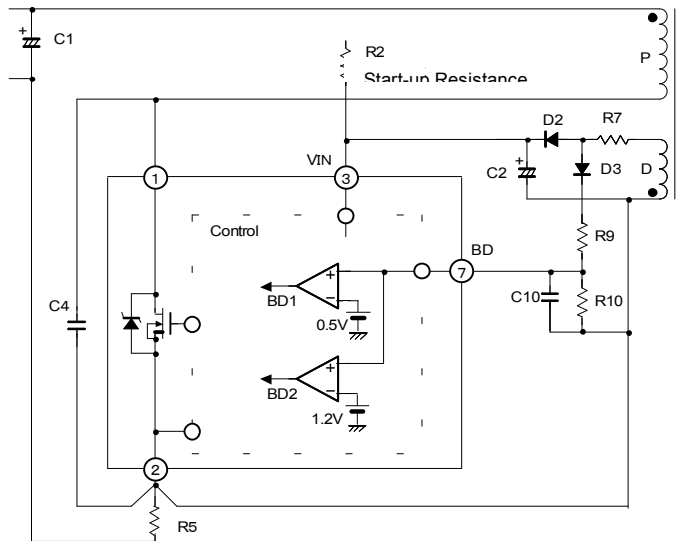


Fig.17. Quasi-Resonant and Delay Circuit

8.4.2 Waveform Input to the BD Terminal and Internal Standard Time

As shown in Fig.18, the transition between the Quasi-Resonant and the Bottom-Skip mode compares T_{B1} and the internal standard time $T_{OFF(MIN1)}/T_{OFF(MIN2)}$. The switching between the normal operations (the Quasi-Resonant and the Bottom-Skip), which will be described later, and the stand-by operation (Auto PRC and the intermittent oscillation) is achieved by comparing T_{B2} and internal standard time $T_{STB(1)}/T_{STB(2)}$.

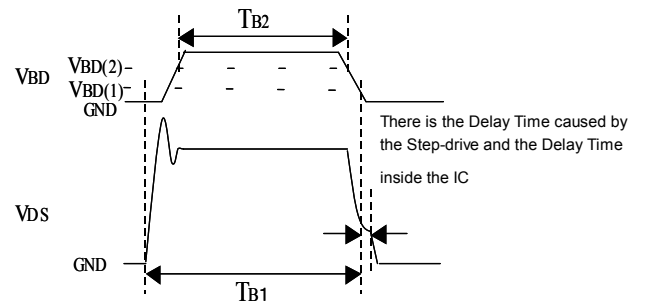
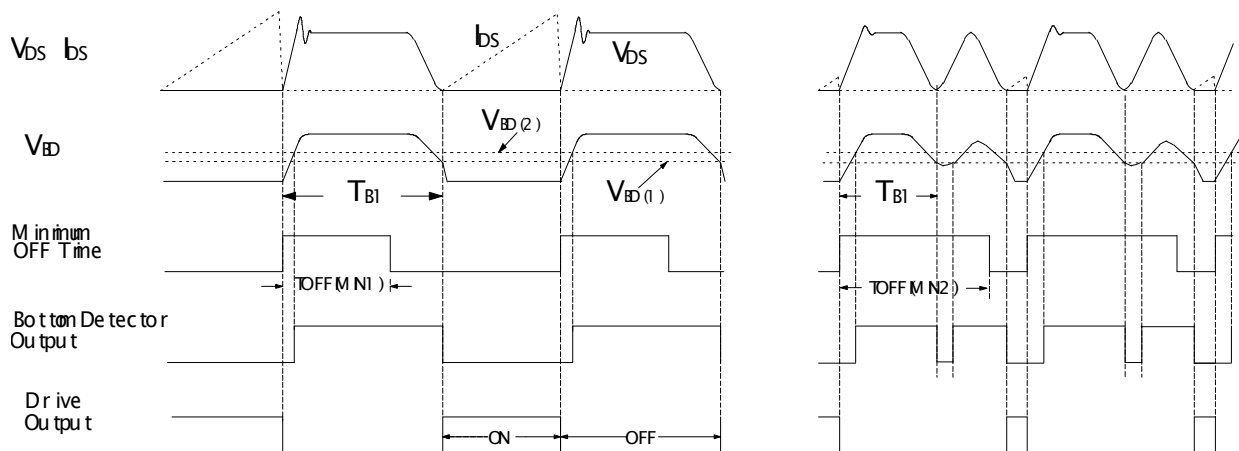


Fig.18. Waveform of BD Terminal Input Vol.

8.4.3 Bottom-Skip Operation

During Bottom-Skip mode, the turn-ON operation is prohibited during $T_{OFF(MIN1)}/T_{OFF(MIN2)}$ which is the internal standard time of the IC. The turn-ON operation is provided when the BD terminal voltage drops lower than $V_{BD(1)}$. The Quasi-Resonant operation (Fig.19(a) and Fig.20) is provided at heavy load, and at light and medium load, the Bottom-Skip operation (Fig.19(b) and Fig.21) skipping V_{DS} is provided.



(a) Heavy load

(b) Light load

Fig.19 Timing Chart of the Bottom-Skip Quasi-Resonant Operation

The switching between Fig.19 (a) and (b) is provided automatically by comparing the internal standard time $T_{OFF(MIN1)}$ or $T_{OFF(MIN2)}$ and T_{B1} . The T_{B1} is described as the time from the MOSFET turn-OFF to the time when the T_{B1} exceeds $V_{BD(2)}$ and drops below $V_{BD(1)}$.

8.4.3.1 Fig.19(a) Quasi-Resonant

T_{B1} becomes longer than $T_{OFF(MIN1)}$ at the Quasi-Resonant point, and when the load becomes lighter than this mode, T_{B1} becomes shorter, as the energy releasing time of the secondary side becomes shorter. Consequently, it switches to the Bottom-Skip mode where T_{B1} becomes shorter than $T_{OFF(MIN1)}$, and the internal standard time switches to $T_{OFF(MIN2)}$ automatically.

8.4.3.2 Fig.19(b) Bottom-Skip

T_{B1} becomes shorter than $T_{OFF(MIN2)}$ at the Bottom-Skip mode, and when the load becomes heavier than this mode, T_{B1} becomes longer, as the energy releasing time of the secondary side becomes longer. Consequently, it switches back to the Quasi-Resonant mode where T_{B1} becomes longer than $T_{OFF(MIN2)}$, and the internal standard time switches

to $TOFF(MIN1)$ automatically.

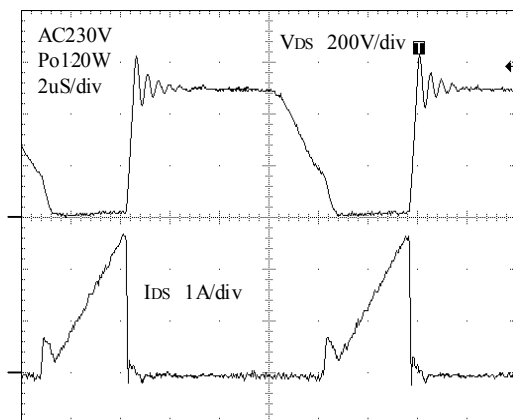


Fig.20 Waveform of Quasi-Resonant

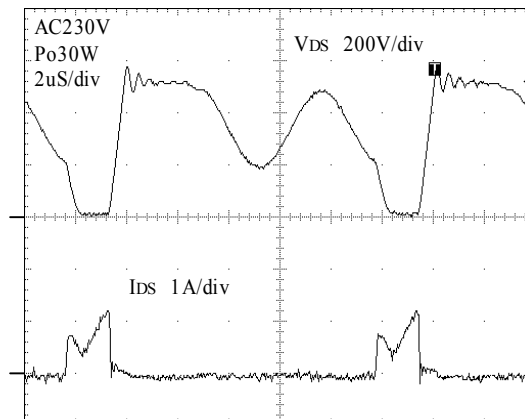


Fig.21 Waveform of Bottom-Skip

As described above, the internal standard time of the IC ($TOFF(MIN1)$, $TOFF(MIN2)$) provides the Hysteresis operation automatically.

8.4.4. Hysteresis Function

The fixed $TOFF(MIN)$ without the Hysteresis function is shown in Fig.24. In this case, with the specific input/output conditions, it may have both the operations of the Bottom-Skip and the Quasi-Resonant. For example, the Bottom-Skip is provided where the load becomes lighter at the Quasi-Resonant operation and $TB1$ becomes shorter than $TOFF(MIN)$, and where the Bottom-Skip is provided, it lowers the oscillating frequency and increases both the OFF-time and the ON-time. As a result, $TB1$ (that appears in next OFF-time) becomes longer, and the Quasi-Resonant mode is provided, and $TB1$ becomes longer than $TOFF(MIN)$ again. As described above, the operation may not be stable with the fixed $TOFF(MIN)$; therefore the bottom may skip or not, and the magnetic noise may be generated from the transformer. In order to avoid such the problems, Hysteresis needs to be added to $TOFF(MIN)$.

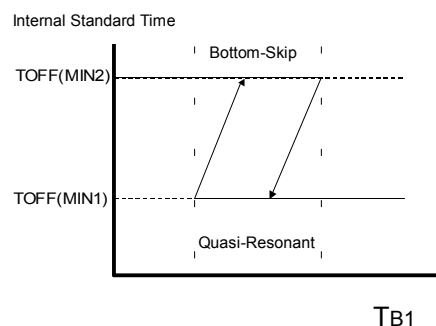


Fig.22. Switching of Operation Mode

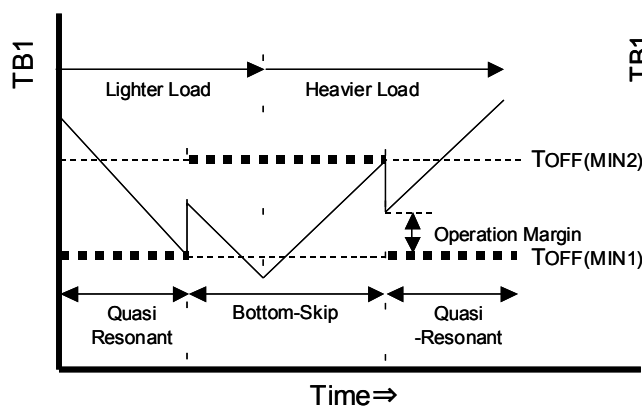


Fig.23. Hysteresis Function

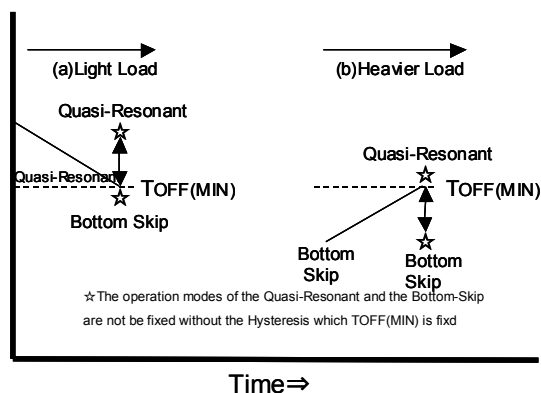


Fig.24. Without Hysteresis Function

As shown in Fig.23, switching to the Quasi-Resonant is prevented by adding this Hysteresis function which makes

$T_{OFF(MIN)}$ from shorter $T_{OFF(MIN1)}$ to longer $T_{OFF(MIN2)}$ when the Quasi-Resonant is switched to the Bottom-Skip. Thus, this mode is stabilized. The operation of switching from Quasi-Resonant from the Bottom-Skip mode is opposite to the above described and provides stable operation. The function of Hysteresis is shown in Fig.22.

As shown in Fig.25, there is a case in which it does not turn ON at the second V_{DS} bottom, and instead turns ON at the third V_{DS} bottom depending on the design of the transformer and the input/output conditions. In this case, the operational mode is not fixed at the switching point of the second and the third V_{DS} bottom, and the second and the third bottom may appear at random. This kind of Hysteresis function is not provided in this series, thus, the IC having $T_{OFF(MIN1)}$ and $T_{OFF(MIN2)}$ and matched to the application is to be used.

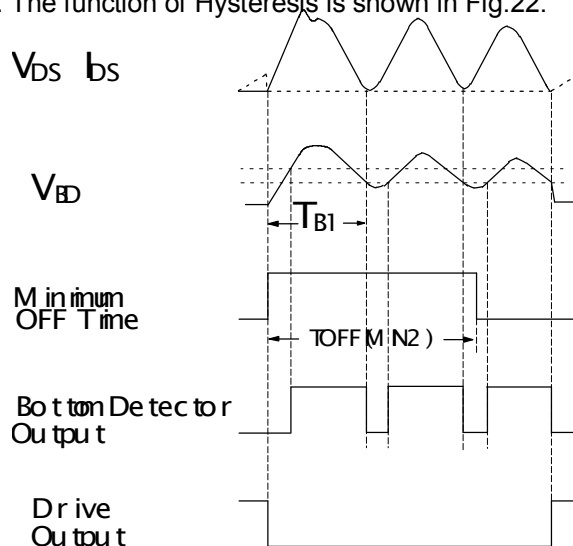


Fig.25. Waveform of Bottom-Skip

8.5 Operation at Stand-By

8.5.1 Switching Time of Stand-by ($T_{STB(1)}/T_{STB(2)}$) Mode and Operation Mode

The STR-X6400 series has two types of built-in stand-by functions to match various load modes. The switching losses cannot be neglected at light load (several % of the load), since the oscillating frequency becomes more than 100kHz even at the Bottom-Skip operation. Therefore, the STR-X6400 series has a built-in Auto PRC function, which controls the ON-time automatically with a fixed OFF-time of 46μsec (≈ 22 kHz), and at the light load (0% to several % of the whole load), as shown in Fig.26. Furthermore, it switches to the intermittent (burst) oscillation at the ultra light load (0% to 0.2% of the whole load), as shown in Fig.27.

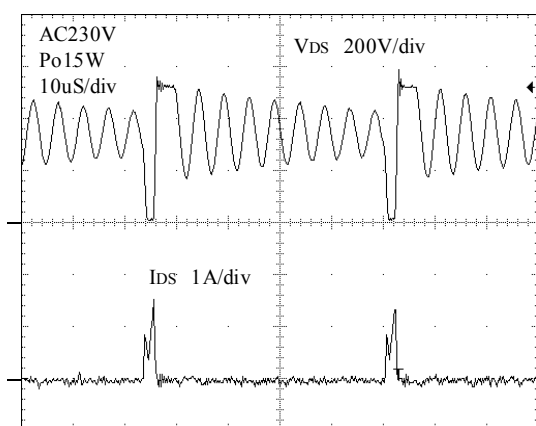


Fig.26. Waveform of PRC Operation

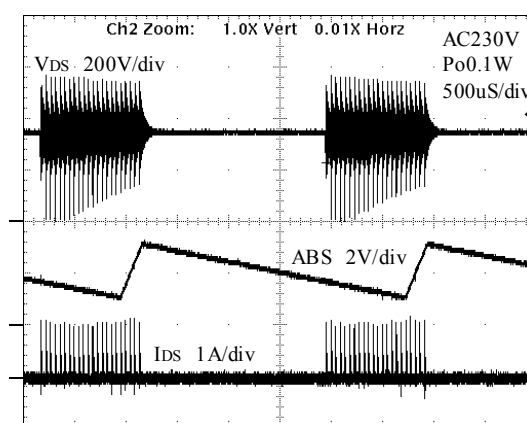


Fig.27. Waveform of Burst Operation

The switching between the normal operation (the Quasi-Resonant and the Bottom-Skip), and the stand-by operation (PRC and burst mode), is determined by comparing the internal standard time for stand-by $T_{STB(1)}/T_{STB(2)}$ of the IC and T_{B2} (refer to Fig.18). As shown in Fig.28, $T_{STB(1)}/T_{STB(2)}$ and $T_{OFF(1)}/T_{OFF(2)}$ depends on independent circuits.

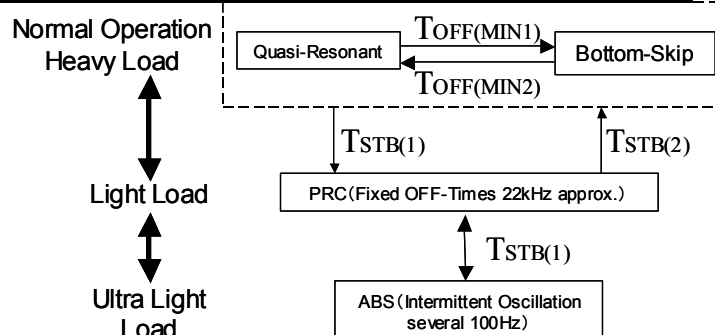


Fig.28. Relationship of Each Operation Mode

8.5.1.1 Normal Operation to PRC Operation

T_{B2} is longer than $T_{STB(1)}$ during the normal operation, and when the load becomes lighter than this mode, T_{B2} becomes shorter, as the energy releasing time of the secondary side becomes shorter. Consequently, it switches to the PRC operation, which will be described later. In this mode, T_{B2} becomes shorter than $T_{STB(1)}$ and the internal standard time switches to $T_{STB(2)}$ automatically.

8.5.1.2 PRC Operation to Normal Operation

T_{B2} is shorter than $T_{STB(2)}$ at the PRC operation, and when the load becomes heavier than this mode, T_{B2} becomes longer, as the energy releasing time of the secondary side becomes longer. Consequently, it switches to the normal operation where T_{B2} becomes longer than $T_{STB(2)}$ and the internal standard time switches to $T_{STB(1)}$ automatically.

As described above, the Hysteresis characteristic applies to $T_{STB(1)}/T_{STB(2)}$ the same as $T_{OFF(MIN1)}/T_{OFF(MIN2)}$. The conditions of each operation (normal: $T_{STB(1)}$, PRC: $T_{STB(2)}$) are held in the internal circuit, until the next T_{B2} is input. During PRC operation, it switches to the intermittent oscillation, since the IC recognizes the mode as the ultra light load, condition of $T_{B2} < T_{STB(1)}$ continues for a certain period.

8.5.2 ABS Terminal (Pin 4) and Intermittent Oscillation

The oscillation circuit for the intermittent (burst) oscillation is incorporated in the STR-X6400 series, and Fig.29 shows the timing chart. Fig.30 shows the circuit diagram during intermittent operation, and Fig.31 shows the flow chart. The capacitor C8 (4700pF to 0.1μF approx.) is to be connected No.4 terminal. The discharging circuit ($I_{ABS(IN)}$) operates continuously at the No.4 terminal, and the charging circuit ($I_{ABS(OUT)}$) operates when the conditions of ultra light load, which will be described later, are satisfied. During ultra light load mode, C8 is charged and discharged, and the intermittent cycle length is determined, and the soft-start is simultaneously provided for the drain current. The ABS terminal should be short-circuited to GND when the intermittent oscillation **feature** is not required.

During ultra light load mode, when T_{B2} becomes shorter (refer to Fig.18) and satisfies the condition of $T_{B2} < T_{STB(1)}$, C8 starts charging ($I_{ABS(OUT)} = 165\mu A(TYP)$). When the ABS terminal voltage rises and reaches 3.1V (TYP), it stops the charging and oscillation ceases. Due to this, it prevents malfunction, since the condition of $T_{B2} < T_{STB(1)}$ is required for a certain period. Furthermore, C8 continues discharging until it reaches $V_{ABSTH(1)} = 1.0V(TYP)$ through the discharging circuit ($I_{ABS(IN)} = 14\mu A(TYP)$) simultaneously as the oscillation is stopped.

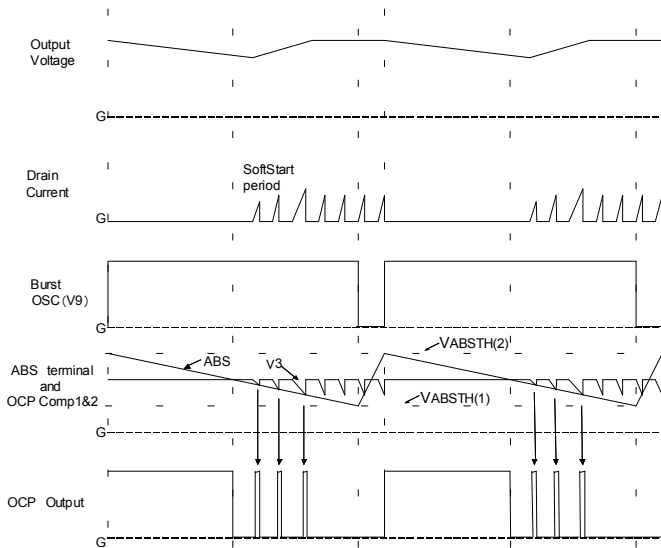


Fig.29. Timing Chart of Intermittent Oscillation

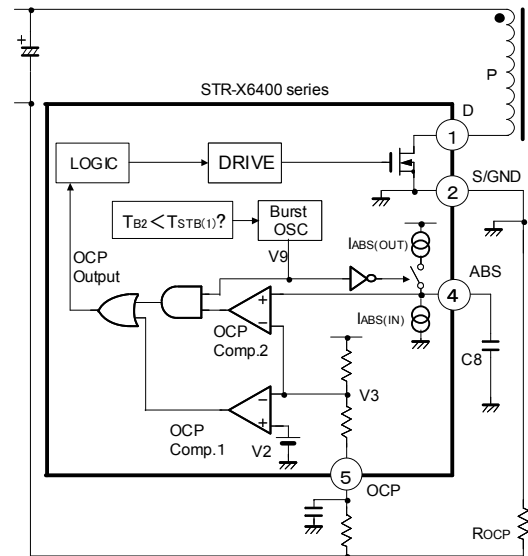


Fig.30. Block Diagram at Intermittent Oscillation

Soft-start is provided when the oscillation starts by making use of the ABS terminal voltage variation that from 3.1V to 1.0V. The Comp.1, which is shown in Fig.30, is the OCP circuit of the MOSFET.

Soft-start operation uses the detecting voltage V_3 generated from the drain current, to minus (-) input of the OCP Comp.2, and the ABS terminal voltage is connected to plus (+) input. The down slope of the C8 becomes the voltage that controls the drain current. Therefore, the drain current is restricted in proportion to the C8 voltage. Consequently, the magnetic noise from the transformer is controlled because of the controlled increase of drain current, as shown in Fig.29.

The intermittent oscillation will occur if the $TB_2 < TSTB(1)$ hold at the time when the ABS terminal voltage is discharged by $V_{ABSTH(1)} = 1.0V(TYP)$. Where the load of secondary side increases and the condition of $TB_2 < TSTB(1)$ is not satisfied, the ABS terminal voltage drops to 0V as it returns to the normal operation. C8 charge level is held by the internal circuit until next TB_2 is generated.

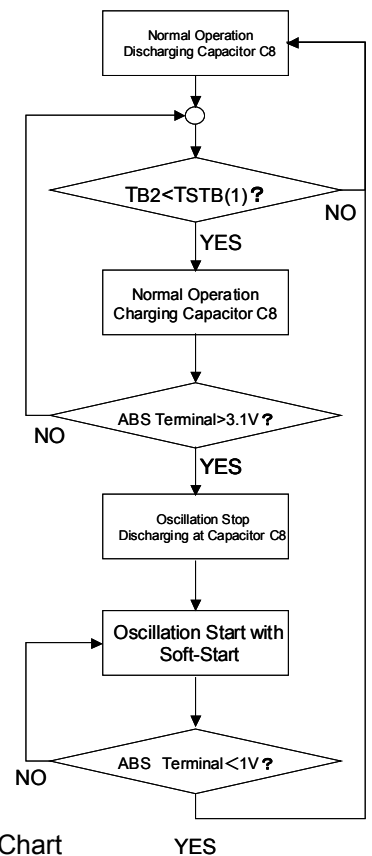


Fig.31. Flow Chart

8.6 Thermal Shutdown Circuit

This circuit that makes the latch operate when the frame temperature of the IC is above **140°C(MIN)**. Since the control IC and the MOSFET are built-in the same package, it also operates with overheating of the MOSFET. In the conventional STR-F6600 series, both the control IC and the MOSFET are mounted on the same frame (substrate), however in the STR-X6400 series, they are mounted in the separated frames. Therefore, the difference of the temperature between the control IC and the MOSFET is to be noted.

8.7 Step-Drive Circuit

The STR-X6400 series reduces turn-On noises by adopting the step-drive circuit for the MOSFET drive circuit as shown in Fig.32.

The drive current at turn-ON is controlled at low current by RG.1 and makes the gate voltage increase gradually, and the gate voltage shall be raised rapidly through Rg.1+Rg.2 after approximately 0.8 μ sec.

The MOSFET drive voltage adopts the constant voltage drive circuit maintaining $V_{DRV}=8.4V_{TYP}$, and it is not affected by V_{IN} . The MOSFET gate charge is discharged rapidly through Rg.3 when the MOSFET is turned OFF.

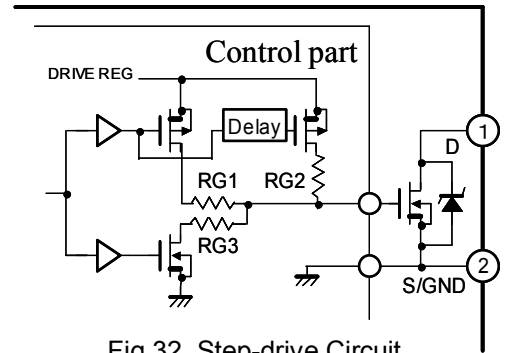


Fig.32. Step-drive Circuit

Consequently, in the STR-X6400 series, the MOSFET gate voltage is switched with a two-step waveform, and this provides an ideal drive, storing the sufficient gate voltage at normal drive by controlling the gate voltage and restricting the surge current flowing at turn-ON.

8.8 Typical Characteristics

The comparison of the conventional STR-F6600 and the STR-X6400 series, for oscillating frequency is shown in Fig.33, and Fig.34 shows its power efficiency. Both series provide the Quasi-Resonant mode at the maximum load; therefore, almost the same oscillating frequency and power efficiency are achieved. However, at medium load, there is a difference in the oscillating frequency and the power efficiency between those two series since the STR-F6600 series provides the Quasi-Resonant, and the STR-X6400 series provides the Bottom-Skip operation. Furthermore, at the ultra light load, because of the fact that the frequency of the STR-F6600 is above 200kHz, and the frequency of the STR-X6400 series provides intermittent oscillation approximately at 300Hz. The intermittent oscillating frequency at that time is approximately 7kHz, which reduces the switching losses considerably.

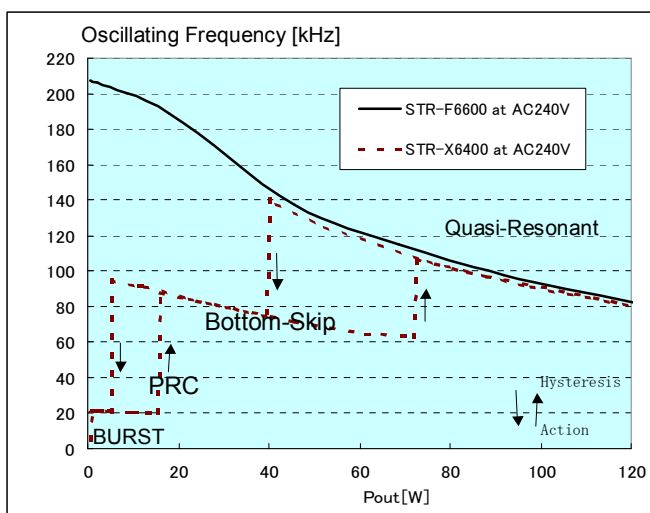


Fig.33. Typical Characteristics of Oscillating Frequency

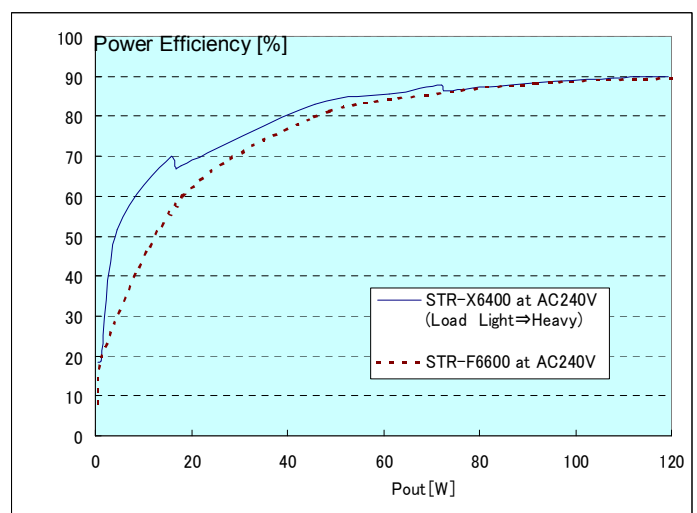


Fig.34. Typical Characteristics of Power Efficiency